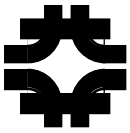

Fermilab

Read Out Electronics for the D0 Upgrade CFT *CFT TRD Section V*

by Fred Borcherding

Overall Design

The CFT read out electronics consists of the front end electronics which are located in the collision hall and the level 2/3 read out electronics which are located in the movable counting house. The front end electronics receives the analog electrical signals from the VLPC cassettes splits them and stores one part of the signal in a 32 deep pipeline buffer. On a level 1 accept one of the stored events is digitized using the SVX-IIe chip and transferred over a fast serial link to the moving counting house. The other part of the analog signal is discriminated using the SIFT-2b chip and the discriminated outputs are used to form a pre level 1 axial track list. This list is transmitted to other detector parts for use in level 1 triggers and is also pipe lined for transmission to the level 2/3 on a level 1 accept.

The front end electronics which includes the digitization and the trigger formation are located on either stereo or trigger boards which are mounted directly on the VLPC cassettes which are located in the center of the detector platform in the collision hall. The first stage in the read out chain is the port cards which are located in the center detector platform but separated from the cassettes. The final stage of the read out are the VME Readout Buffers, VRB, located in the moving counting house. Figure 1 below shows the basic parts of the read out system. The port card boards and VRBs are identical to those used by the silicon readout system and share the same crates and support infrastructure.

Interface to VLPC cassette

Each cassette holds two PC boards which are slightly different versions of the same board. The board mounted on the right side of the cassette when viewed from the front is called the Right Hand Board, RHB, and the one on the

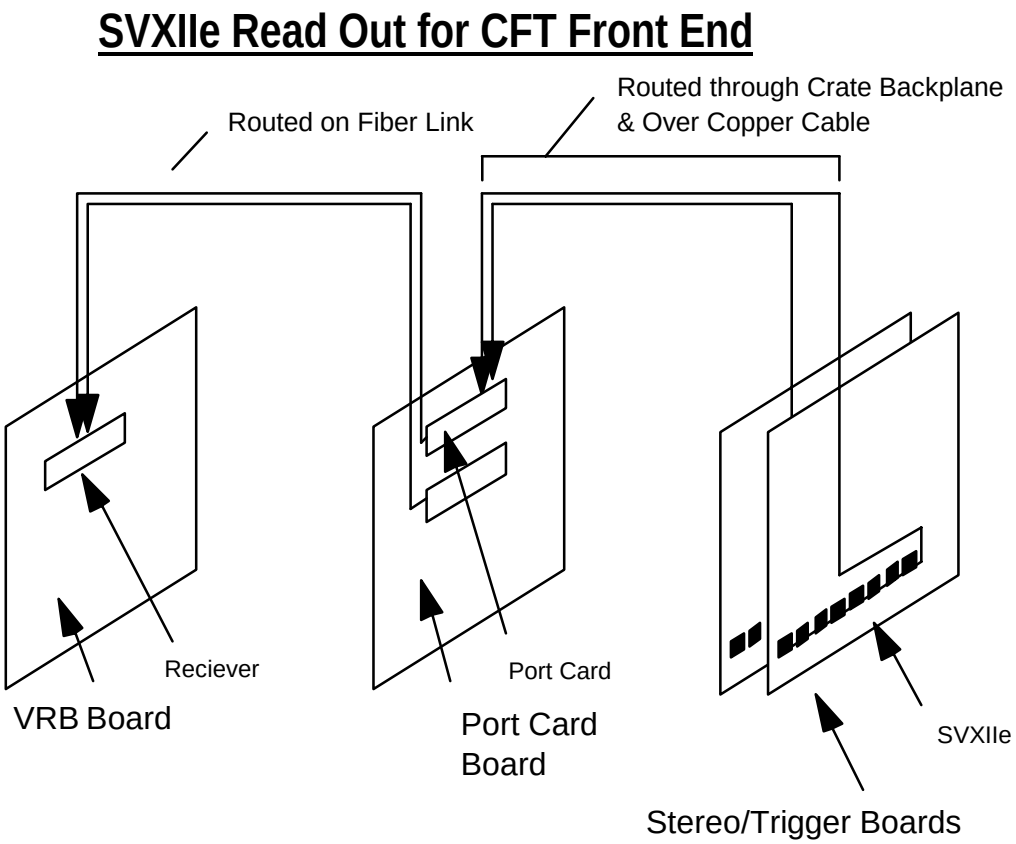

Figure 1: Overall layout of the read out system. The analog signals are digitized in the SVX IIe chips located on the stereo/trigger boards on the right. The digitized and zero suppressed data is read out of the chain of SVXs by a port card located on the port card board via a copper link. The data is then transferred to a VRB in the moving counting house over a fast serial link.

left the Left Hand Board, LHB. Each PCB supports 512 channels of signal from the cassette. The RHB but not the LHB will interface the cryogenic power and controls system for each cassette. Each PCB will interface the bias voltage supply and return for the VLPCs. Eighty boards are called stereo boards and are used to read out the stereo fibers. Another eighty boards are called trigger boards and are used to read out the axial fibers. The trigger boards also contain the logic which forms the level 1 axial trigger tracks. While each board supports 512 input channels the CFT will not use them all. The remaining channels are used by the CPS. On each stereo board 448 channels are used by the CFT and on each trigger board 480 channels are used.

The signal connection between PCB and the cassette is made along the bottom edge of the board. See figure 2. Along this bottom edge are located eight sets of pads which mate to the high density connector pins of the Synapse connector. Each of these eight sets includes 64 pads which are the single ended signal outputs from the VLPCs. These are also the return lines for the VLPC bias current and are all DC coupled through a resistor to a common VLPC bias return. Each of these lines is also AC coupled through an isolation

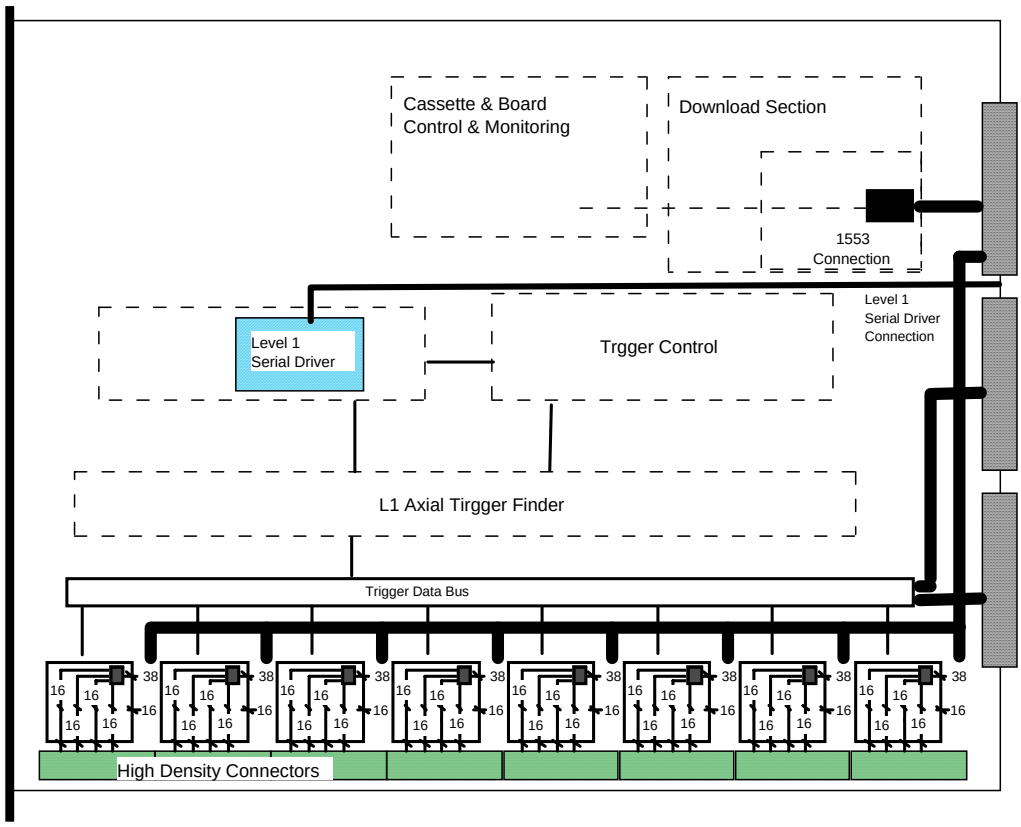

Figure 2: Schematic of a front end board trigger boards for the CFT. The blocks along the bottom edge are the pad arrays which mate with the Synapse connectors. Directly above them are the eight multi-chip modules, MCM, each of which contains four SIFT-2b chips and one SVXIIe chip.

capacitor to the input of the front end electronics. Eight of the pads are connected to a common VLPC bias supply which supplies the bias current to the VLPCs. Six of the pads are connected to the cryogenic controls for the cassette.

Front End Electronics

All the channels in a cassette will be either axial fibers or stereo fibers. This is done to accomidate the trigger which uses only the axial fibers. The front end electronics is also different for the axial and stereo channels. The axial channels have a digital pick off for use in the trigger and the stereo channels do not.

All the channels are digitized in an SVX chip. The axial channels are modified by placing a digital pick off in the analog line before the SVX.

Digital Pick off for Trigger

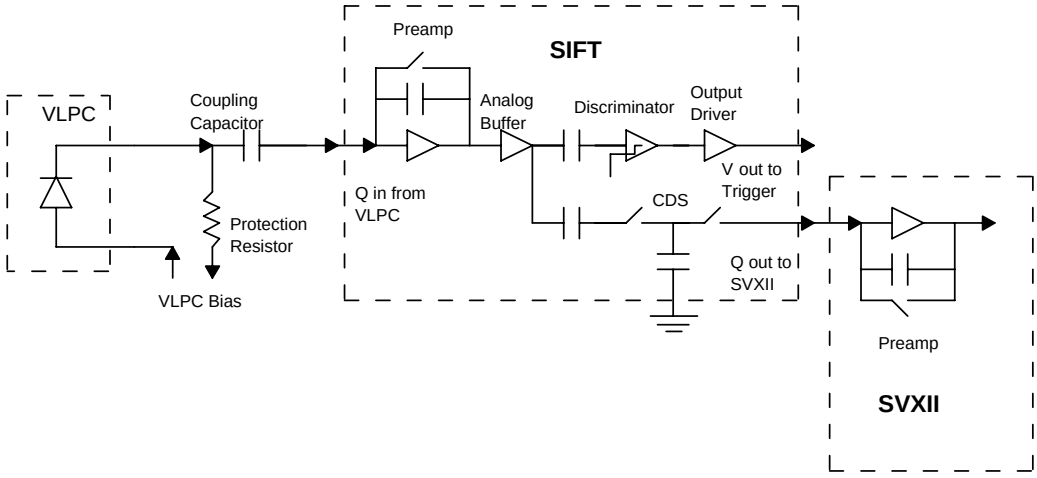

Figure 3: Electronics schematic for one channel of the trigger board. The VLPC is represented by the small box on the left. The analog signal is separated from the bias current by the coupling capacitor. This capacitor is a discrete part mounted on the PCB. The next two boxes represent the circuit inside the SIFT-2b chip and the first part of the SVXIIe chip respectively.

SVXII Readout

The SVXII chip and its read out support were designed for the silicon tracker but are well suited to the fiber read out as well. The signal amplitude and shape as well as the effective detector capacitance out of the VLPC are well within the range of the SVXII chip. While eight bits of digitized amplitude may not be strictly necessary for the fiber channels there are considerable savings in development and maintainance by sharing the readout for the 78,000 channels of the CFT with the over 300,000 channels of the D0 silicon vertex tracker. Detailed information on the silicon tracker read out system can be found in several places and will not be repeated here. The following will repeat some of the general features and highlight the differences for the fiber system.

The SVXII read out system has three parts. The first part is the digitization part which is the SVXII chip itself. This is connected via copper bus to the port card which is the read out part. This in turn is connected via fast optiacal link to the VME Buffer Driver, VBD, which collects and stores the data for VME based readout. The SVXII chips are located on the front end PCBs. The portcards are located in a separate set of crates in the platform among the portcards for the silicon tracker. The VBDs are located in the movable counting house, again among those for the silicon tracker.

Each PCB will have eight SVX chips. Each of these chips will have ½ of its 128 input channels connected to VLPC outputs. The SVXII chips are read out in chains of chips. When a level 1 accept is received all the chips stop accuring data and transfer the data form one of their analog memories to the digitization stage. When the first SVX on a chain has finished its digitization it starts transmitting data to the port card. After the first SVX has finised its data transmission the next chip in the chain is free to transmit its own. Since the SVX

chips will be run in zero suppression mode only those fibers for which the signal was above a threshold will be read out. Thus the total read out time is a factor of the occupancy of the fibers for each of the chips in a chain. Given the expected occupancy for the CFT and the readout time the eight SVX chips on each PCB are arranged into two chains.